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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,898	09/24/2003	Cyril Cabral JR.	YOR920030469US1	2246

7590 07/01/2005

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EXAMINER	
WILSON, CHRISTIAN D	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,898	CABRAL ET AL.	
	Examiner	Art Unit	
	Christian Wilson	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *16-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 16 – 30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on November 1, 2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong *et al.* in view of Buynoski.

Chong *et al.* (US 6,624,489) teaches a method of fabricating a CMOS FET comprising the steps of providing a substrate **10**, providing a polysilicon layer **18** formed on a gate dielectric **16**, forming a polysilicon gate electrode [column 4, line 4], doping the polysilicon layer with a dopant [column 4, lines 20-25], depositing a metal and an alloy **30** on the gate electrode, and siliciding the gate electrode to form a silicide **62** adjacent to the gate dielectric layer. Chong *et al.* teaches forming the gate electrode and then doping the polysilicon layer. Buynoski (US 6,518,113) teaches doping the polysilicon layer and then forming the gate electrode [Figures 5

and 6]. It would have been obvious to one of ordinary skill in the art to use the process of Buynoski in the method of Chong *et al.* since Buynoski teaches that doping and then forming the gate electrode provides superior electrical performance and reliability [column 13, lines 35-50].

Regarding claim 2, Chong *et al.* further teaches performing the doping step after the forming step [column 4, line 4].

Regarding claims 3, 5, and 6, Chong *et al.* further teaches a doping process with ion implantation of B, As, or P with a dose of $5E10^{14}$ to $1E10^{16}$ atoms/cm^2 [column 4, line 22].

Regarding claim 4, Chong *et al.* teaches using B, As, or P as a dopant, but not Sb. Buynoski teaches B, As, P, or Sb as a dopant [column 12, lines 1-10]. It would have been obvious to one of ordinary skill in the art to use Sb as a dopant since Buynoski teaches that Sb is an equivalent material choice and therefore is well known as a substitute for B, As, or P.

Regarding claims 7 and 8, Chong *et al.* further teaches amorphizing the polysilicon gate electrode by ion implanting Si or Ge [column 4, lines 50-60].

Regarding claims 9 – 12, Chong *et al.* further teaches a metal of Ni or Co and an alloy of Pt [column 4, line 65].

Regarding claims 13 – 14, Chong *et al.* further teaches a siliciding process of annealing between 250° C and 900° C for 5 sec to 1 hr [column 6, lines 22-23].

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong *et al.* and Buynoski as applied to claim 13 above, and further in view of Vaidya *et al.*

Chong *et al.* as modified by Buynoski teaches the limitations of claim 13 as described above, but does not teach forming at least one monolayer of dopant at the interface of the gate dielectric layer and silicide. Vaidya *et al.* (*Effect of dopant implantation on the properties of*

$TaSi_2$/poly-Si composites) teaches an annealing process where at least one monolayer of dopant is formed at the interface of the dielectric and silicide [Figure 2]. It would have been obvious to one of ordinary skill in the art that the method of Chong *et al.* would provide the interface layer of dopant described by Vaidya *et al.* since the annealing processes are the same [pg. 846, 2nd col., 3rd para.]. Further, Vaidya *et al.* teaches that this process provides improved electron mobility [sect. IVB] and work function [sect. IVC].

Response to Arguments

5. Applicant's arguments filed April 18, 2005 have been fully considered but they are not persuasive.

Applicant argues that Chong *et al.* as modified by Buynoski does not teach a silicide adjacent to the gate dielectric layer. This argument is not persuasive since this limitation is disclosed as described in the preceding rejection. Further, the words of a claim must be given their "plain meaning" unless they are defined in the specification. While the claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. *In re* American Academy of Science Tech Center, ___ F.3d___, 2004 WL 1067528 (Fed. Cir. May 13, 2004). The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320,

1322 (Fed. Cir. 1989); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004). Ordinary, simple English words whose meaning is clear and unquestionable, absent any indication that their use in a particular context changes their meaning, are construed to mean exactly what they say.

In this instance, the plain meaning of "adjacent" is met by the teachings of Chong *et al.* as modified by Buynoski. Adjacent has the plain meaning of not distant or nearby (taken from Merriam-Webster's Collegiate Dictionary, 10th edition). Since no special definition is provided in the specification to define "adjacent" as meaning "touching" or "next to", the plain meaning is used during examination.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gopinath *et al.* teaches a gate silicidation technique where the entire polysilicon gate is consumed by the silicide.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian Wilson whose telephone number is (571) 272-1886. The examiner can normally be reached on weekdays, 7:30 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian Wilson, Ph.D.
Primary Examiner
Art Unit 2891

CDW